This listing of claims will replace all prior versions of claims in the application.

Claim 1. (currently amended) A method for depositing multiple metal layers on a semiconductor microchip wafer substrate, comprising:

(a) contacting a semiconductor microchip wafer substrate with an electrolytic plating composition, the plating composition comprising:

(i) a copper metal source and

(ii) a second metal source distinct from the (i) copper metal source and that is chosen from among zinc, tantalum, beryllium, magnesium, titanium, tin, palladium, silver, cadmium ~~cadium~~, or a copper alloy that comprises one or more of zinc, tantalum, beryllium, magnesium, titanium, tin, palladium, silver and cadmium ~~cadium~~;

(b) electrolytically depositing a first metal layer of copper, from the copper metal source, on the semiconductor microchip wafer substrate at a first reduction potential;

(c) electrolytically depositing a second metal layer, from the second metal source, on the semiconductor microchip wafer substrate at a second reduction potential at least 0.2 V different ~~distinct~~ from the first reduction potential,

wherein the first metal layer functions as an electrical circuit, and the second metal layer ~~yacr~~ functions as an insulator layer.

Claim 2. (original) The method of claim 1 wherein the first metal layer is a substantially homogenous copper metal layer.

Claim 3. (original) The method of claim 1 wherein the second metal layer is a copper alloy.

Claims 4-6. (cancelled)

Claim 7. (previously presented) The method of claim 1 wherein a plurality of first metal layers are deposited with a plurality of alternating second metal layers.

Claims 8-31. (cancelled)